2122

ATTORNEY'S DOCKET NO: **S1022.80278US00**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	David Alan Edwards, et al.
Serial No:	09/411,792
Confirmation No:	8808
Filed:	October 1, 1999
For:	INTERFACE FOR TRANSFERRING DEBUG INFORMATION
Examiner:	Ted T. Vo
Art Unit:	2122

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document and the listed enclosures are being placed in the United States mail with first-class postage attached, addressed to the Board of Appeal and Interferences, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450, on September 18, 2006.

Gail Driscoll
Signature

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P. O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' BRIEF PURSUANT TO 37 C.F.R. §41.37

James H. Morris, Reg. No. 34,681
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210
(617) 720-3500
Attorneys for Appellants

TABLE OF CONTENTS

This brief is in furtherance of the Notice of Appeal mailed on April 14, 2006 and received by the PTO on April 17, 2006. In accordance with 37 C.F.R. §1.8(a), the deadline for submission of this appeal brief under 37 C.F.R. §41.37(a)(1) with a three month extension of time is September 17, 2006. Because September 17, 2006 falls on a Sunday, the deadline for submission is extended, under 37 C.F.R. §1.7, to September 18, 2006. A check for the fee required under 37 C.F.R. §41.20(b)(2) is submitted herewith.

I. REAL PARTY IN INTEREST (37 C.F.R. §41.37(c)(1)(i))

The real party in interest in this application is the assignee, ST Microelectronics Limited, a corporation having a place of business at 1000 Aztec West, Almondsbury, Bristol BS12 4SQ, United Kingdom.

II. RELATED APPEALS AND INTERFERENCES (37 C.F.R. §41.37(c)(1)(ii))

There are no other appeals or interferences known to the Appellants, the Appellants' legal representative, or the assignee which will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS (37 C.F.R. §41.37(c)(1)(iii))

There are 64 total claims currently pending in this application (i.e., claims 1-64), of which four are independent, and sixty are dependent. Each of claims 1-64 stands rejected and each of these claims is appealed. The appealed claims are set forth in Appendix A. The status of each of the claims is summarized in the list below:

1. Rejected and Appealed: Claims 1-64
2. Allowed: None
3. Withdrawn: None
4: Objected To: None
5. Canceled: None

IV. STATUS OF AMENDMENTS (37 C.F.R. §41.37(c)(1)(iv))

No amendments have been filed subsequent to the Final Office Action mailed November 14, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER (37 C.F.R.§41.37(c)(1)(v))

In one aspect, the invention relates generally to an interface for transferring debug information for debugging a processor. (Specification, page 1, lines 6-7). System-on-chip devices are devices that include a processor, one or modules, bus interface, memory devices, and one or more system buses for communicating information on a single chip (Specification, page 1, lines 10-12). Because communications between modules occur internally to the chip, accessing this information to diagnose hardware or software problems presents challenges. (Specification, page 1, lines 12-15).

A non-limiting example of one embodiment described in Applicants' specification is provided below. As shown in Figure 1, integrated circuit 101 includes a processor 102 and a debug circuit 103, coupled by a system bus 105 (Specification, page 7, lines 2-5) System bus 105 may be, for example, a conventional processor bus, packet switch, or other communication medium used to communicate operating information between modules of device 101 (Specification, page 7, lines 5-7). Communication link 104 couples processor 102 to debug circuit 103, and is separate from system bus 105 (Specification, page 7, lines 20-21). Communication link 104 is configured to transfer debug information from processor 102 to debug circuit 103, and to transfer state and processor control information from the debug circuit 103 to processor 102 (Specification, page 7, lines 23-25). The information sent from the processor to the debug circuit may include, for example: operand address information may be included in the information transferred between the processor and the debug circuit (Specification, page 10, lines 6-10); an operand value (Specification, page 7, lines 23-25); a program counter value (Specification, page 8, lines 30-33); a status indicating that a computer instruction in the writeback stage is a valid instruction (Specification, page 9, lines 4-5); a status indicating that a computer instruction in the writeback stage is a first instruction past an executed

branch instruction (Specification, page 9, lines 6-8); a status indicating a type of the executed branch instruction (Specification, page 9, lines 14-16); and/or process identifier information of an executed instruction (Specification, page 9, line 31 – page 10, line 3).

Claim 1

Claim 1 is directed to a microcomputer comprising a processor and a debug circuit. The processor and the debug circuit may be coupled by a communication link, which is used by the processor to transmit information about the state of the processor, including at least an operand address that indicates a memory location at which an operand value is stored.

Claim 21

Claim 21 is directed to a microcomputer on a single integrated circuit, comprising a processor and a debug circuit. The processor and the debug circuit may be coupled by a communication link, which is used by the processor to transmit information about the state of the processor, including at least one of: an operand address that indicates a memory location at which an operand value is stored and an operand value. The processor is further configured to transmit to the debug circuit a program counter value, a status indicating that a computer instruction in the writeback stage is a valid instruction, a status indicating that a computer instruction in the writeback stage is a first instruction past an executed branch instruction, a status indicating a type of the executed branch instruction, and process identifier information of an executed instruction.

Claim 22

Claim 22 is directed to a microcomputer comprising: at least one processor; a debug circuit; a system bus; and means for transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor including at least an operand address that indicates a memory location at which an operand value is stored.

The limitation of claim 22 reciting a "means for transmitting" is a means-plus-function limitation and its corresponding structure is described in numerous locations in the specification, including, for example, page 7, lines 20-26 and the description accompanying element 104 of Figure 1; page 8, lines 24-29 and the description accompanying element 215 of Figure 2; page 12, lines 1-8 and the description accompanying element 313 of Figure 3; page 14, lines 4-5, and the description accompanying element 420 of Figure 4.

Claim 42

Claim 42 is directed to a method of transferring information between a processor and a debug circuit over a communication link. The method comprises: transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor including at least one operand address that indicates a memory location at which an operand value is stored; and transmitting a program counter value indicating the program counter of the processor.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R.§41.37(c)(1)(vi))

The sole ground of rejection to be reviewed on appeal is the rejection of claims 1-64 under 35 U.S.C. §102(b) as purportedly being unpatentable over U.S. Patent No. 5,737,516 (hereinafter "Circello").

VII. ARGUMENT (37 C.F.R. §41.37(c)(1)(vii))

As discussed above, claims 1-64 stand rejected by the Office Action mailed November 14, 2006 under 35 U.S.C. §102(b) as purportedly being unpatentable over Circello. This rejection is improper, as Circello fails to disclose all of the limitations of the independent claims.

A. Discussion of Circello

Figure 1 of Circello shows a data processing system 5 that includes a processing core 9 and a debug module 10. As shown in Figure 1, several signals are transmitted from the processing core 9 to the debug module 10. A Bus Grant signal may be transmitted from processing core 9 to debug module 10 which is used by CPU 2 of processing core 9 to indicate to debug module 10 that it has been granted use of K-Bus 25 (Col. 29, lines 41-55). Further, a CPU Processor Status (CPST) signal may be transmitted from processing core 9 to debug module 10 that indicates the type of operation currently being executed by data processor 3 (Col. 18, lines 47-53). For example, the CPST signal may indicate when execution of an instruction begins, when execution of an instruction should continue, when data processor 3 enters into a selected mode of operation, when a preselected branch instruction is executed, and when operation of data processor 3 is halted (Col. 18, lines 53-60).

Additionally, several signals may be transmitted from processing core 9 to debug module 10 over K-Bus 25 (Col. 4, lines 62-63). The signals transmitted over K-Bus 25 are KADDR, KDATA, and KCONTROL (Col. 4, lines 63-65). The KADDR signal is used to send instruction addresses accessed during normal operation of data processor 3 to debug module 10 and the KDATA signal is used to send operand values to debug module 10 (col. 18, lines 25-31). Circello does not explicitly disclose how the KCONTROL signal is used.

In summary, in the system of Circello there are five signals transmitted from processing core 9 to debug module 10 (Bus Grant, CPST, KADDR, KDATA, and KCONTROL). Circello discloses that these signals are used to transmit information such as CPU status, instruction addresses, and operand values.

Nowhere does Circello disclose or suggest that operand addresses are sent to debug module 10 via these signals. Further, Circello does not disclose or suggest that the processing core 9, debug module 10, and K-bus 25 are all implemented on a single integrated circuit.

B. Circello Does Not Disclose Transmitting An Operand Address From A Processor To A Debug Circuit

During the lengthy prosecution of this application, Applicants have repeatedly pointed out that Circello does not disclose transmitting an operand address from processor core 9 to debug circuit 10. Rather, Circello discloses only five signals that are transmitted from processor core 9 to debug module 10 (i.e., Bus Grant, CPST, KADDR, KDATA, and KCONTROL).

Applicants emphasize that Circello does not disclose or suggest that any of the signals sent from processor core 9 to debug module 10 include an operand address. Although the KADDR signal may include instruction addresses, instruction addresses are very different from operand addresses. That is, an instruction address specifies the memory location of an instruction stored in memory, whereas an operand address specifies the memory location of an operand value stored in memory.

During prosecution, the Examiner argued that an instruction address could possibly point to an instruction that includes operand values. The Examiner argued that the instruction address could be considered an operand address because the operand values would be stored at the memory location identified by the instruction address. The Examiner argued that, as a result Circello discloses, transmission of operand addresses from processor core 9 to debug module 10. *See* Office Action mailed November 14, 2005, page 3, lines 1-11. In response, Applicants pointed out that Circello does not disclose or suggest that instructions include operand values and that the Examiner has cited nothing to support this asssertion. *See* Applicants' response mailed February 14, 2006, page 3, lines 19-25. Based on the Examiner's remarks in the Advisory Action mailed March 23, 2006, the Examiner appears to have withdrawn this position.

Applicants also acknowledge that the KDATA signal of the system of Circello permits operand values to be transmitted from the processor core to the debug module. However, an operand value is very different from an operand address. That is, an operand address is the memory location in which an operand value is stored.

Moreover, the Examiner no longer appears to contend that Circello discloses an operand address being transmitted from the processor core 9 to the debug module 10. Rather, the Examiner takes the position that because Circello discloses certain types of data being transferred from the processor core to the debug circuit, all types of data being transferred from the processor core to the debug circuit are disclosed.

Specifically, in the Examiner's comments accompanying the Advisory Action mailed March 23, 2006, the Examiner states:

> Applicants tend to address repeatedly the data, "operand address" as the patentability. It should be noted that "data" as in the claim read from the specification, is only information. And also, this data, "operand address" in the claim does not thing, and just a mere data.
>
> As noted that, Applicants have repeatedly argued the debug circuit in Circello does not receive "data", so called operand address. However, in the prior action, Examiner, indicated that, one can include in data, "operand address", operator address, address of other instruction or data per se, etc. in a trace array. A claim cannot seek for a protection to the type of data that is stored in an opened an public domain like a trace circuit, discussed in the debug circuit of Circillo, for example, Circillo addresses.

Thus, the Examiner appears to admit that Circello does not disclose or suggest that an operand address is transmitted from processor core 9 to debug circuit 10. Rather, the Examiner has taken the improper view that because Circello discloses transmitting "data," and, in particular, CPU status, instruction addresses, and operand values, Circello has disclosed transmitting all types of data between the processor core and debug circuit 10.

This view is improper, as it well established that, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Vendegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Further, "[t]he identical invention must be shown in as complete detail as is contained in the...claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Here, the Examiner does not appear to contest the fact that a claim limitation (i.e., the transmission of an operand address from a processor to a debug circuit) is not shown, nor does the Examiner contend that this limitation is inherent in the prior art (as it is clearly not). If a claim limitation is not shown in the prior art, the claim cannot be anticipated.

C. Circello Does Not Disclose The Use Of A Single Integrated Circuit

Circello does not disclose that the processor core and debug circuit are included on a single integrated circuit (IC). Rather, Circello merely states that data processor 3 in Figure 1 includes, *inter alia*, a core 9 and a debug module 10 (column 4, lines 7-10). Circello does not disclose whether these elements are implemented on a single IC, on multiple ICs, or in some other different way.

D. The Claims Patentably Distinguish Over Circello

1. Claims 1-20

Claim 1 is directed to a microcomputer comprising: at least one processor; a debug circuit; a system bus coupling the processor and debug circuit; and a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least an operand address that indicates a memory location at which an operand value is stored.

As should be clear from the discussion above, Circello does not disclose or suggest "a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor **including at least an operand address that indicates a memory location at which an operand value is stored.**"

Thus, claim 1 patentably distinguishes over Circello. Claims 2-20 depend from claim 1 and are patentable for at least the same reasons. Accordingly, it is respectfully requested that the rejections of claims 1-20 be reversed.

2. Claim 21

Claim 21 is directed to a microcomputer implemented on a single integrated circuit. The microcomputer comprises: at least one processor; a debug circuit; a system bus coupling the processor and debug circuit; and a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least one of: an operand address that indicates a memory location at which an operand value is stored; and an operand value. The processor is further configured to transmit to the debug circuit: a program counter value indicating the program counter of the processor at a writeback stage of a pipeline of the processor; a status indicating that a computer instruction in the writeback stage is a valid computer instruction; a status indicating that the computer instruction in the writeback stage is a first instruction past an executed branch instruction; a status indicating a type of the executed branch instruction; and process identifier information of an executed instruction.

As should be clear from the discussion above, Circello does not disclose or suggest a microcomputer **implemented on a single integrated circuit** that includes at least one processor; a debug circuit; a system bus coupling the processor and debug circuit; and a communication link coupling the processor and debug circuit.

Thus, claim 21 patentably distinguishes over Circello. Accordingly, it is respectfully requested that the rejection of claim 21 be reversed.

3. Claims 22-41

Claim 22 is directed to a microcomputer comprising: at least one processor; a debug circuit; a system bus coupling the processor and debug circuit; and means for transmitting to the

debug circuit a plurality of bit values each representing a state of an operation in the processor including at least an operand address that indicates a memory location at which an operand value is stored.

As should be clear from the discussion above, Circello does not disclose or suggest means for transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor **including at least an operand address that indicates a memory location at which an operand value is stored**.

Thus, claim 22 patentably distinguishes over Circello. Claims 23-41 depend from claim 22 and are patentable for at least the same reasons. Accordingly, it is respectfully requested that the rejections of claims 22-41 be reversed.

3. Claims 42-64

Claim 42 is directed to a method for transferring information between a processor and a debug circuit over a communication link. The method comprises: transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor including at least an operand address that indicates a memory location at which an operand value is stored; and transmitting a program counter value indicating the program counter of the processor.

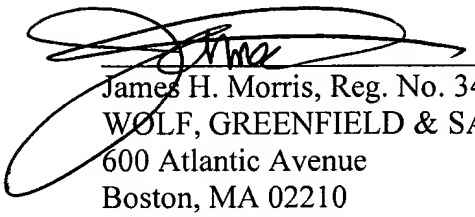
As should be clear from the discussion above, Circello does not disclose or suggest, transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor **including at least an operand address that indicates a memory location at which an operand value is stored.**

Thus, claim 42 patentably distinguishes over Circello. Claims 43-64 depend from claim 42 and are patentable for at least the same reasons. Accordingly, it is respectfully requested that the rejections of claims 42-64 be reversed.

VII. CONCLUSION

For the foregoing reasons, the rejection of claims 1-64 is improper and should be reversed.

Respectfully submitted,



James H. Morris, Reg. No. 34,681
WOLF, GREENFIELD & SACKS, P.C.
600 Atlantic Avenue
Boston, MA 02210
Tel: (617) 720-3500
Attorneys for Appellants

Attorney Docket No.: S1022.80278US00
Dated: September 18, 2006

APPENDIX A – CLAIMS AS PENDING

1. (Previously Presented) A microcomputer comprising:

at least one processor;

a debug circuit;

a system bus coupling the processor and debug circuit; and

a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least an operand address that indicates a memory location at which an operand value is stored.

2. (Original) The microcomputer according to claim 1, wherein at least one of the plurality of bit values represents a state of an operation in the processor including an operand value and operand address.

3. (Original) The microcomputer according to claim 1, wherein the processor is further configured transmit to the debug circuit a program counter value indicating the program counter of the processor.

4. (Original) The microcomputer according to claim 3, wherein the program counter has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the processor.

5. (Original) The microcomputer according to claim 4, wherein the processor is further configured transmit to the debug circuit a status indicating that a computer instruction is in the writeback stage is a valid computer instruction.

6. (Original) The microcomputer according to claim 4, wherein the processor is further configured transmit to the debug circuit a status indicating that the computer instruction in the writeback stage is a first instruction past a branch instruction.

7. (Original) The microcomputer according to claim 6, wherein the processor is further configured transmit to the debug circuit a status indicating a type of an executed branch instruction.

8. (Original) The microcomputer according to claim 7, wherein the debug circuit is configured to transmit a trace packet indicating the type of the executed branch instruction.

9. (Original) The microcomputer according to claim 1, wherein the plurality of bit values representing a pre-execution state of the processor.

10. (Original) The microcomputer according to claim 1, wherein the processor is configured to suppress transmitting the plurality of bit values upon detecting an exception.

11. (Original) The microcomputer according to claim 1, wherein the processor is further configured transmit to the debug circuit address information of an executed instruction.

12. (Original) The microcomputer according to claim 1, wherein the processor is further configured transmit to the debug circuit data information of an executed instruction.

13. (Original) The microcomputer according to claim 1, wherein the processor is further configured transmit to the debug circuit process identifier information of an executed instruction.

14. (Original) The microcomputer according to claim 1, wherein the debug circuit is capable of transmitting processor control signals, including at least one of:

a signal to suspend operation of the processor;

a signal to resume fetching instructions;

a signal to reset the processor;

a signal to indicate that an exception has occurred in the debug unit.

15. (Original) The microcomputer according to claim 1, wherein at least one of the plurality of bit values represents a match state between a match value and a portion of an executed instruction.

16. (Original) The microcomputer according to claim 1, wherein at least one of the plurality of bit values represents a match state between a match value and a memory address accessed by the processor in response to an executed instruction.

17. (Original) The microcomputer according to claim 1, wherein the processor is further configured transmit to the debug circuit a value indicating an increment of the program counter of the processor.

18. (Original) The microcomputer according to claim 1, wherein the processor is further configured transmit to the debug circuit a value indicating a change in process identifier value.

19. (Original) The microcomputer according to claim 3, wherein the debug circuit is adapted to generate trace information including the program counter.

20. (Original) The microcomputer according to claim 1, wherein the microcomputer is implemented on a single integrated circuit.

21. (Previously Presented) A microcomputer implemented on a single integrated circuit, the microcomputer comprising:

at least one processor;

a debug circuit;

a system bus coupling the processor and debug circuit; and

a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a plurality of bit values each representing a state of an operation in the processor including at least one of:

an operand address that indicates a memory location at which an operand value is stored; and

an operand value;

wherein the processor is further configured transmit to the debug circuit:

a program counter value indicating the program counter of the processor at a writeback stage of a pipeline of the processor;

a status indicating that a computer instruction is in the writeback stage is a valid computer instruction;

a status indicating that the computer instruction in the writeback stage is a first instruction past an executed branch instruction;

a status indicating a type of the executed branch instruction; and

process identifier information of an executed instruction.

22. (Previously Presented) A microcomputer comprising:

at least one processor;

a debug circuit;

a system bus coupling the processor and debug circuit; and

means for transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor including at least an operand address that indicates a memory location at which an operand value is stored.

23. (Original) The microcomputer according to claim 22, wherein at least one of the plurality of bit values represents a state of an operation in the processor including an operand value and operand address.

24. (Original) The microcomputer according to claim 22, wherein the microcomputer further comprises means for transmitting to the debug circuit a program counter value indicating the program counter of the processor.

25. (Original) The microcomputer according to claim 24, wherein the program counter has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the processor.

26. (Original) The microcomputer according to claim 25, wherein the processor comprises means for transmitting to the debug circuit a status indicating that a computer instruction is in the writeback stage is a valid computer instruction.

27. (Original) The microcomputer according to claim 25, wherein the processor comprises means for transmitting to the debug circuit a status indicating that the computer instruction in the writeback stage is a first instruction past a branch instruction.

28. (Original) The microcomputer according to claim 27, wherein the processor comprises means for transmitting to the debug circuit a status indicating a type of an executed branch instruction.

29. (Original) The microcomputer according to claim 28, wherein the debug circuit includes means for transmitting a trace packet indicating the type of the executed branch instruction.

30. (Original) The microcomputer according to claim 22, wherein the plurality of bit values representing a pre-execution state of the processor.

31. (Original) The microcomputer according to claim 22, wherein the processor includes means for suppressing a transmission of the plurality of bit values upon detecting an exception.

32. (Original) The microcomputer according to claim 22, wherein the processor further comprises means for transmitting to the debug circuit address information of an executed instruction.

33. (Original) The microcomputer according to claim 22, wherein the processor includes means for transmitting to the debug circuit data information of an executed instruction.

34. (Original) The microcomputer according to claim 22, wherein the processor comprises means for transmitting to the debug circuit process identifier information of an executed instruction.

35. (Original) The microcomputer according to claim 22, wherein the debug circuit comprises means for transmitting processor control signals, including at least one of:

a signal to suspend operation of the processor;

a signal to resume fetching instructions;

a signal to reset the processor;

a signal to indicate that an exception has occurred in the debug unit.

36. (Original) The microcomputer according to claim 22, wherein at least one of the plurality of bit values represents a match state between a match value and a portion of an executed instruction.

37. (Original) The microcomputer according to claim 22, wherein at least one of the plurality of bit values represents a match state between a match value and a memory address accessed by the processor in response to an executed instruction.

38. (Original) The microcomputer according to claim 22, wherein the processor includes means for transmitting to the debug circuit a value indicating an increment of the program counter of the processor.

39. (Original) The microcomputer according to claim 22, wherein the processor is further configured transmit to the debug circuit a value indicating a change in process identifier value.

40. (Original) The microcomputer according to claim 22, wherein the debug circuit includes means for generating trace information including the program counter.

41. (Original) The microcomputer according to claim 22, wherein the microcomputer is implemented on a single integrated circuit.

42. (Previously Presented) A method for transferring information between a processor and a debug circuit over a communication link, the method comprising:

transmitting to the debug circuit a plurality of bit values each representing a state of an operation in the processor including at least an operand address that indicates a memory location at which an operand value is stored; and

transmitting a program counter value indicating the program counter of the processor.

43. (Original) The method according to claim 42, wherein at least one of the plurality of bit values represents a state of an operation in the processor including an operand value.

44. (Original) The method according to claim 43, wherein the program counter has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the processor.

45. (Original) The method according to claim 44, the method further comprises a step of transmitting to the debug circuit a status indicating that a computer instruction is in the writeback stage is a valid computer instruction.

46. (Original) The method according to claim 44, the method further comprising a step of transmitting to the debug circuit a status indicating that the computer instruction in the writeback stage is a first instruction past a branch instruction.

47. (Original) The method according to claim 46, the method further comprising a step of transmitting to the debug circuit a status indicating a type of an executed branch instruction.

48. (Original) The method according to claim 47, the method further comprising a step of transmitting a trace packet indicating the type of the executed branch instruction.

49. (Original) The method according to claim 42, wherein the plurality of bit values representing a pre-execution state of the processor.

50. (Original) The method according to claim 42, the method further comprising a step of suppressing a transmission of the plurality of bit values upon detecting an exception.

51. (Original) The method according to claim 42, the method further comprising a step of transmitting to the debug circuit address information of an executed instruction.

52. (Original) The method according to claim 42, the method further comprising a step of transmitting to the debug circuit data information of an executed instruction.

53. (Original) The method according to claim 42, the method further comprising a step of transmitting to the debug circuit process identifier information of an executed instruction.

54. (Original) The method according to claim 42, the method further comprising a step of transmitting processor control signals, including at least one of:

a signal to suspend operation of the processor;

a signal to resume fetching instructions;

a signal to reset the processor;

a signal to indicate that an exception has occurred in the debug unit.

55. (Original) The method according to claim 42, wherein at least one of the plurality of bit values represents a match state between a match value and a portion of an executed instruction.

56. (Original) The method according to claim 42, wherein at least one of the plurality of bit values represents a match state between a match value and a memory address accessed by the processor in response to an executed instruction.

57. (Original) The method according to claim 42, the method further comprising a step of transmitting to the debug circuit a value indicating an increment of the program counter of the processor.

58. (Original) The method according to claim 42, the method further comprising a step of transmitting a value indicating a change in process identifier value to the debug circuit.

59. (Original) The method according to claim 42, the method further comprising a step of generating trace information including the program counter.

60. (Original) The method according to claim 42, wherein the microcomputer is implemented on a single integrated circuit.

61. (Previously Presented) The microcomputer of claim 1, wherein the plurality of bit values further includes at least an instruction address.

62. (Previously Presented) The microcomputer of claim 21, wherein the plurality of bit values further includes at least an instruction address.

63. (Previously Presented) The microcomputer of claim 22, wherein the plurality of bit values further includes at least an instruction address.

64. (Previously Presented) The method of claim 42, wherein the plurality of bit values further includes at least an instruction address.